Instructions for Pro Tune Up 4 v 17 Labs

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Lab 1 Single Driver – Single Receiver

Open Lab_1_Basic_Loop.ffs

Please view the video for instructions → **http://www.screencast.com/t/JjvYDBYkMqyS**

Show circuit and explain source of models, show stack-up and explain how to modify stack-up,

Run un-terminated simulation & point out ringing, excessive current, and EMI

Add source serial terminating resistor and run the terminated simulation & point out reduced ringing, reduced current, and reduced EMI

Goal of exercise…Introduce LineSim, (Free Form Schematic Editor, Stack-up Editor, Model Library, Ringing Simulation and EMI simulation) and explain that this is a holistic problem. Adding termination to fix Ringing also reduces current and EMI resulting in a more reliable more easily manufactured system

Lab 2 Daisy Chain

Open Lab_2_Daist_Chain.ffs

Please view the video for instructions → **http://www.screencast.com/t/iVJbsEEpEm**

Simulate circuit with no termination. Note the high current and overshoot.

Add source serial termination resistor. Note reduced ringing and reduced current. Explain signal shape at each probe point. Question…What is the width of the valid sampling window for each of the receivers? Question…does this seem like a good strategy?

Remove source serial termination resistor and add an AC parallel load termination. Simulate the circuit. Note that the loading is so heavy that the voltage at the receivers will not swing rail to rail. There is too much loading for the driver.

Reduce the trace length and increase the interconnect impedance until the simulation looks reasonable.

Goal of the exercise is to understand source termination vs load termination and their ramifications on signal shape and driver loading.

Lab 3 Cross Talk

Open Lab3_Cross_Talk.ffs

Video Instructions → **http://www.screencast.com/t/mkeZ6mE1Mi**

Open circuit and simulate non-terminated example at 1H spacing. Note that cross talk is horrible.

Change the spacing between traces to 3H. Note that cross talk is better, but still too much in light of the noise budget.

Move the spacing back to 1H, narrow the traces to 4 mils resulting in 63 ohm impedance rather than 52 ohms at 6 mil width, then add 55 ohm source serial terminating resistors. Note that after the initial transition the cross talk drops to a very acceptable level.

Lab 5 Bi-Directional SDRAM Data with center resistor

Open Lab5_Bi_Dir. Video Instructions → http://www.screencast.com/t/MxXOiG6QL

Simulate the circuit left to right, then simulate the circuit right to left. Observe the time of flight, overshoot, EMI, and signal current as a function of termination resistor value, location, and overall total length of the line. Is there a practical solution which can be physically routed to insure a time of flight and signal settle above Vih or below Vil for a total time of flight and settle is 1.1nS or less? Part B. If you duplicate the circuit and create cross talk regions that would be only 4 mils separation between traces on the two longest transmission lines, how much cross talk will appear at the point the signal would probably be sampled. Here we are guessing at a window that is plus or minus 100 pS from where the clock should be. If you see a problem, how can it be fixed.

Lab 6 Six layer board, Power Integrity, Signal Via By-Passing, and Plane Noise

The video for this lab is on **http://www.screencast.com/t/r8QQXDurtxri**

Open Lab_6_6L_WP_Lab.ffs There are 25 0.1uF 0402 capacitors arrayed across the 4" high by 6" wide six layer PCB. Please investigate the setup so you understand the board stack-up, I encourage you to watch the video and then use that as the base line to change things and do your own experiments to see the effects of capacitors, termination, and spacing on signal quality, and plane noise.

Lab 8 Eight layer board, Signal Via By-Passing, IC Power By Passing, and Plane Noise as a function of capacitor number, value, and position as well as a function of the ground to ground stitching vias.

Open Lab_8_8L_CP_Lab.ffs Video for Lab 8 http://www.screencast.com/t/xUkqjjt5I

What you see is a Signal Integrity schematic on the top and a Power Integrity representation on the bottom. There are two IC's with a single power pin for each IC. These are U1.1 and U2.1. The naming of pins between the top and the bottom windows are independent. I manipulated them to be similar to make the instructions easier. If we were using BoardSim (where data comes from PCB layout system as opposed to LineSim where data comes from your imagination) the reference designator numbers and pins would match.

There are 25 0.1nF 0402 capacitors and a Voltage Regulator Module in the lower left corner.

There are two sets of vias. V1-V4 goes from Top to Layer 3. V2-V3 goes from Top to Bottom. In the case of V2-V3, V3 is relatively close to a set of capacitors where the ground pins on those capacitors form a return current path between Layer 2 Ground and Layer 7 Ground. In the case of V2 there are no vias connecting Layer 2 Ground and Layer 7 Ground within an inch or so. Hence when you look at the performance of V2 compared to V3, you will find V2 displays some very bad behavior above 1GHz.

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