

SI EMC Jump Start 3.0 Class Description
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Designers need to predict the effect of critical layout decisions in order to make a high speed digital system perform properly.

These decisions include:

- Layer Stack-up
- Routing Topology & Termination
- Trace Width and Space Width as a function of layer stack-up
- Power Delivery Design, By-pass Capacitor Selection, Placement, and Connection
- Component Selection and Placement
- Multiple or Split Power / Ground Plane Strategies
- Filtering
- Shielding

Of the 7 items listed above, at least 5, and arguably all 7 of those items must be analyzed and specified prior to beginning layout. Jump Start III teaches the student how to analyze the design and make rational decisions that will result in a right the first time design.

Specific Class Topics Include

1.

How to analyze PC board stack-up?

A board stack-up has two main functions. First, it provides controlled impedance layer pairs for routing the high speed signals. Secondly, it is the only source of the high quality low inductance capacitance which is necessary to bypass the higher frequency components of the driver current. If the stack-up is inadequate for the frequencies involved, the odds of making the design work reliably and also pass regulatory tests become quite remote.

2.

How to design a power deliver system?

A typical 32 bit power delivery system must be capable of supplying impulse current of nearly an amp with frequency components extending above 1 GHz. It is critical to understand how power supplies, bulk capacitors, chip capacitors, embedded capacitance combine to provide a low impedance power deliver system. A poor bypass capacitor strategy can result in both faulty data and / or the radiated emissions which can prevent you from shipping and otherwise fully functional product. Crowding identical capacitors into a small region (like directly under a BGA) can result in power delivery impedance poles. **Key issue....If the bypass capacitor strategy works, ground bounce is reduced, common mode noise is reduced, cross talk is reduced, and EMI is reduced..** In essence we teach a rational process to design a power deliver system which will meet a specific set of design goals.

3.

How to route High Speed Digital Signals

High Speed Digital Signals behave like RF or Microwave signals. Attempting to route these traces without understanding the correct routing techniques can result in a host of problems. These include faulty data, poor manufacturing yield, high warranty return rate, and failing FCC & CISPR regulatory tests. Ringing can actually burn out a circuit. The student must be acutely aware of the return current path. This may require additional components simply to provide a proper path for the return current. With out proper attention to return current paths, signal integrity tools can and will give and overly optimistic predictions of the circuit performance.

4.

Understanding Clock and Buss Topology and Termination Issues.

Clocks must provide clean monotonic edges and minimum skew for the rest of the system to work properly. Busses must settle below the specified noise margin before the set up time and remain below that level through the hold time. The student will learn how to analyze a variety of common problems which must be solved through the proper use of routing topology and signal termination.

5.

Understanding the Jump Start Method

The Jump Start method means planning for success and then performing the critical acts necessary to guarantee that success. The basic steps are as follows:

- A. Triage the signals and set budgets for timing, SI, and EMI.
- B. Design a layer stack up and power delivery system which can support those targets
- C. Analyze each signal type and derive layout rules that will enable that signal type to meet the budget. Here we are taking a detailed look at ringing, cross talk, EMI, and ground bounce. We must analyze routing topology and termination to assure that the design rules given to the layout designer will result in a viable system.
- D. Route the board and perform an “as built” simulation to verify that the layout will meet budgeted goals.
- E. Perform an exhaustive cross talk analysis of the finished “as built” design to make sure energy from a high speed signal is not being coupled on to status type signal causing it to become an unwanted source of EMI or of functional errors.

6.

Applying the Jump Start Method to 8 or more layer boards

The 8 layer board is our friend. It provides sufficient layers to make the analysis for success very straight forward. There are two high speed routing pairs with a nice power ground sandwich (ie..a high quality low inductance capacitor) in the middle. This is the stack-up for minimum design time and maximum guaranteed results.

7.

Applying the Jump Start Method to 6 layer boards.

Six layer boards offer good high speed routing pairs, but sacrifice the power ground sandwich. Hence, six layer boards require careful power deliver system attention or they can fail in a number of aggravating ways.

8.

Applying the Jump Start Method to 4 layer boards.

The 4 layer board has all of the power deliver problems of the six layer board. In addition, every routing via must be analyzed to determine where the return current for each high speed signal is flowing. Incorrectly analyzing even one signal can result in either functional or regulatory failure.

9.

Applying the Jump Start Method to 2 layer boards

Two layer boards are the worst of all worlds. We will address how one synthesizes a power delivery structure and return current plane to support modest digital system.

10.

Understanding EMI generation in the light of common design trade-off's

This section specifically addresses EMI as a primary topic while surveying all of the design decisions on a global basis.

11.

Strategies for Dealing with Multiple Power Supplies

Almost every design has multiple power supplies. The student will learn how to address this issue in the light of high speed signal requirements.

12.

Strategies for dealing with mixed Analogue and Digital Systems

Note 1: Due to the amount of material to be covered in this class, the student must view the video prior to attending the class. This assures the instructor that everyone is using a common terminology and has a common baseline of knowledge from which to build. The class introduction video is available to anyone who wishes to down load and view it.

Note 2: We supply laptop computers for the labs in the class. These machines have laptop type mouse pads. Any student who does not like that type of mouse is invited to bring their own USB type mouse to class.

Note 3: We offer an optional post class open book test for any who wish to receive a certificate of accomplishment. Anyone wishing to take the test must email tfox@siemc.com. Once the test is returned and graded, the student will receive both a .pdf version of the certificate via email and a physical certificate via snail mail. This process generally takes a couple of weeks unless special arrangements are made.